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**Shin**(10) **Pub. No.: US 2015/0243715 A1**(43) **Pub. Date: Aug. 27, 2015**(54) **ORGANIC LIGHT EMITTING DISPLAY  
DEVICE**(52) **U.S. CL.**  
CPC ..... **H01L 27/3248** (2013.01); **H01L 27/3276**  
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**Publication Classification**(51) **Int. Cl.**  
**H01L 27/32** (2006.01)(57) **ABSTRACT**

An organic light emitting display device includes: a display panel including data lines, scan lines, a first power voltage line supplying a first power voltage, and pixels, a pixel of the pixels including: a driving transistor configured to control a drain-to-source current flowing from a first electrode of the driving transistor to a second electrode of the driving transistor according to a voltage at a gate electrode of the driving transistor; an organic light emitting diode (OLED) configured to emit light in accordance with the drain-to-source current; and a first transistor having a gate electrode coupled to a scan line of the scan lines, a first electrode coupled to the second electrode of the driving transistor, and a second electrode coupled to the gate electrode of the driving transistor, the first power voltage line being between the second electrode of the first transistor and an anode of the OLED.

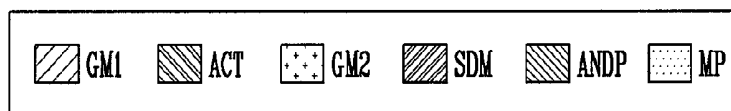
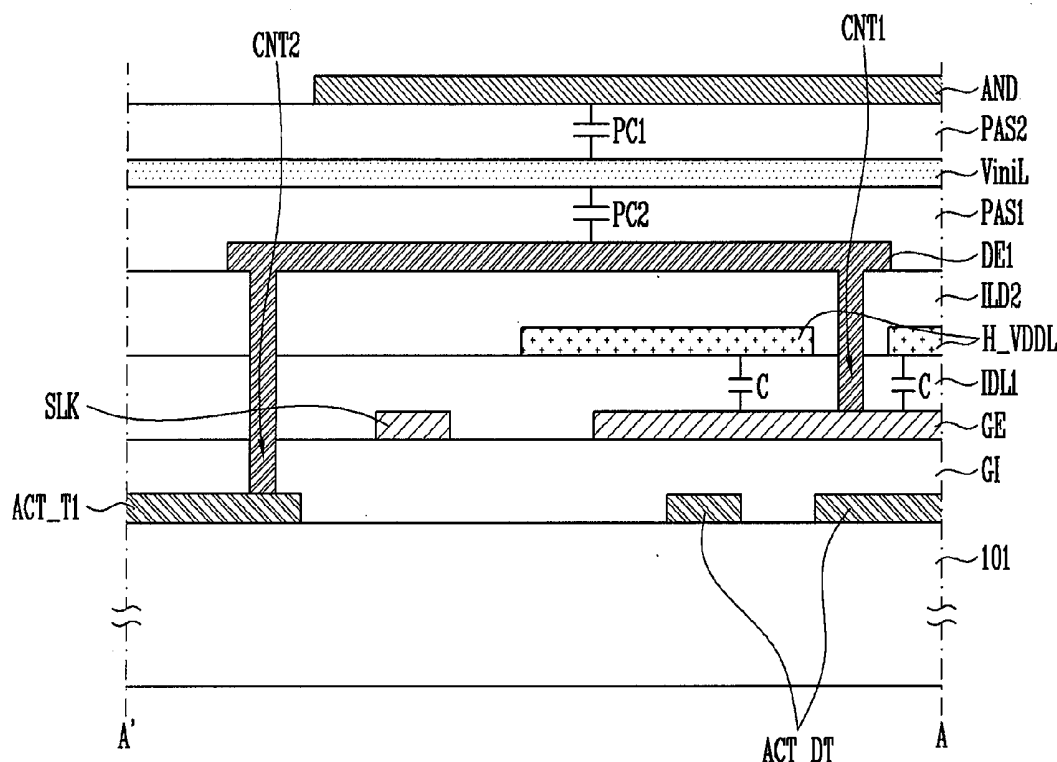


FIG. 1

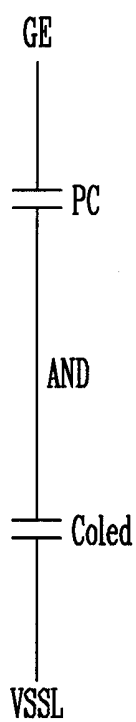


FIG. 2

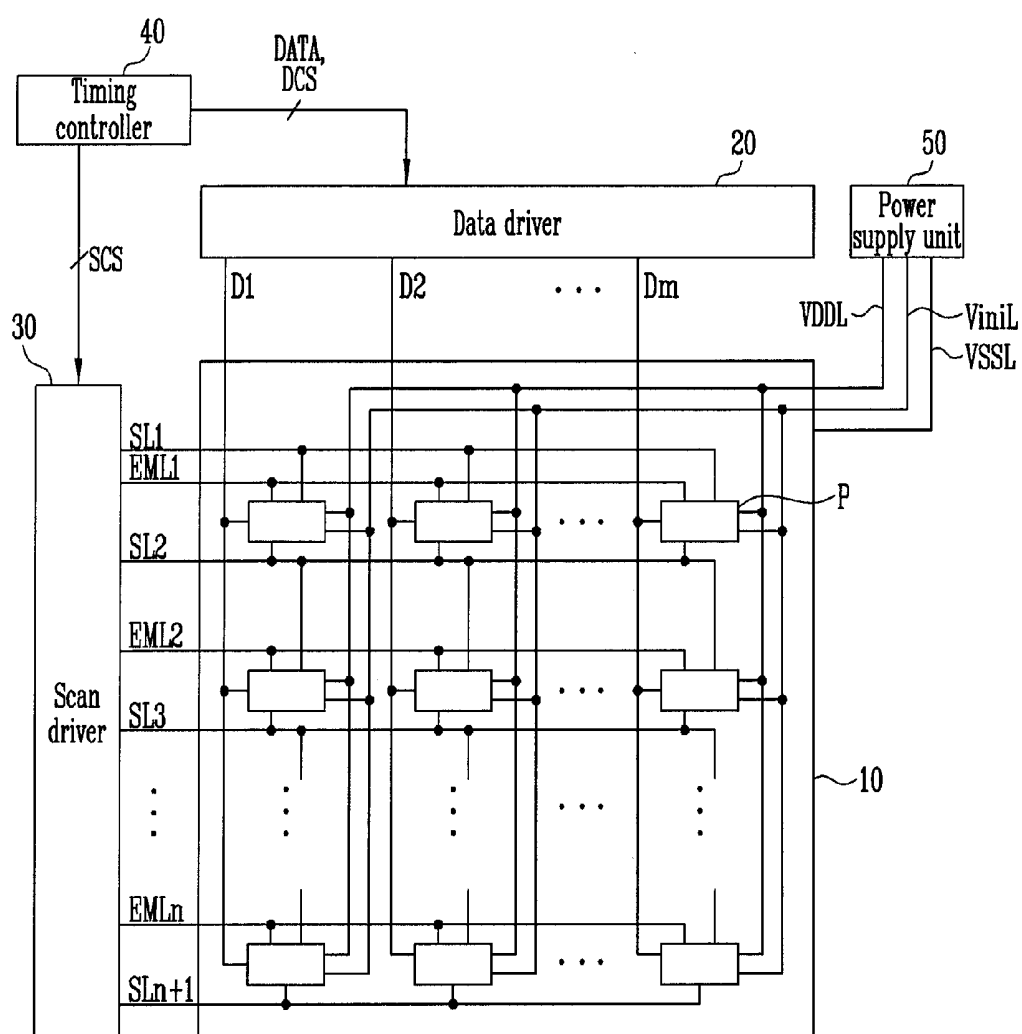


FIG. 3

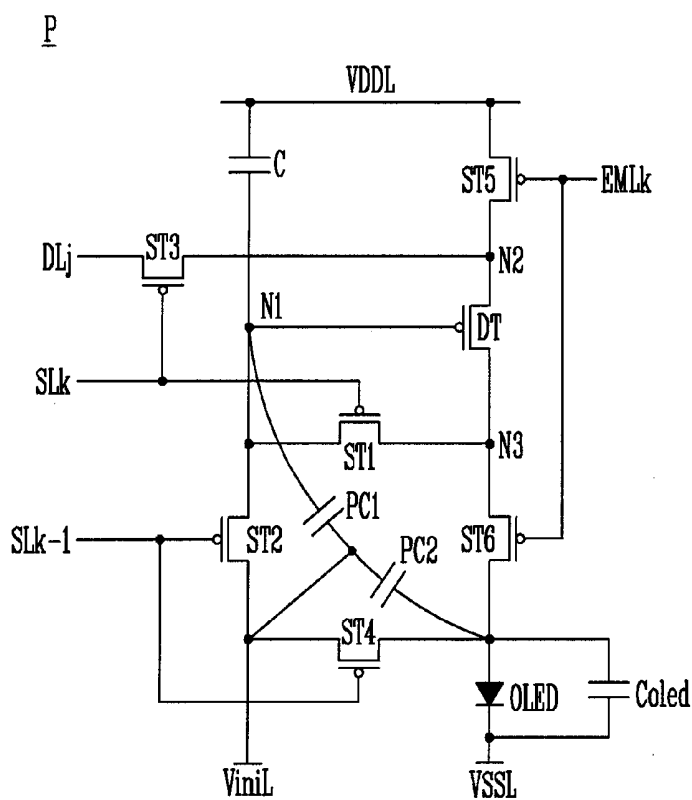


FIG. 4

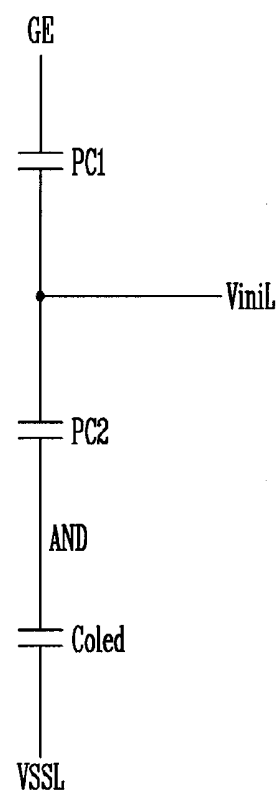


FIG. 5

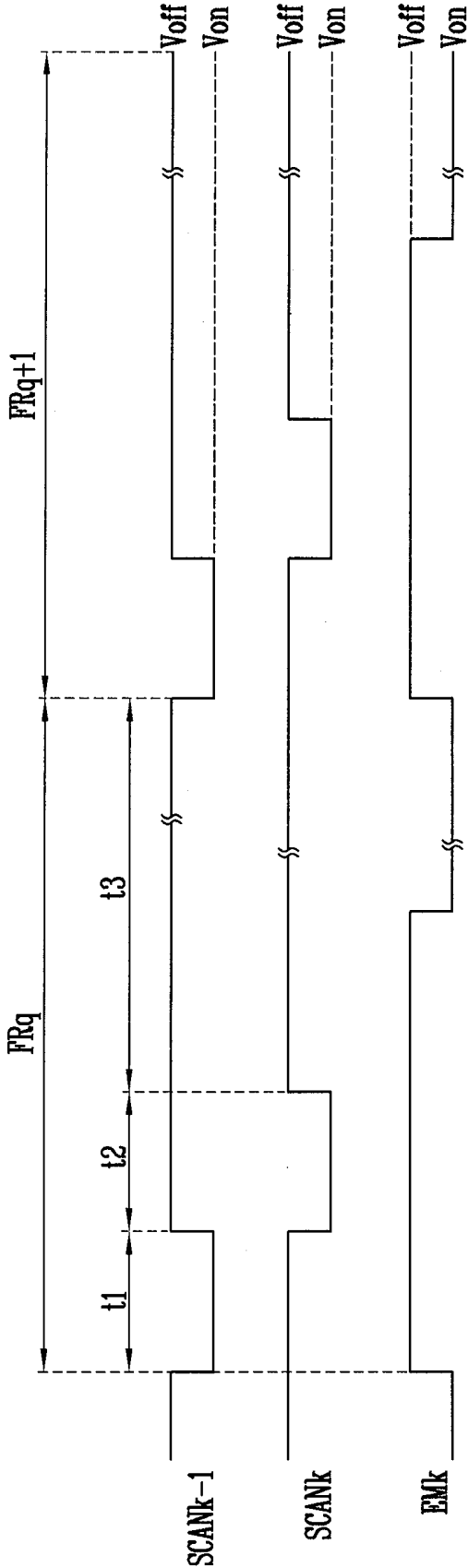
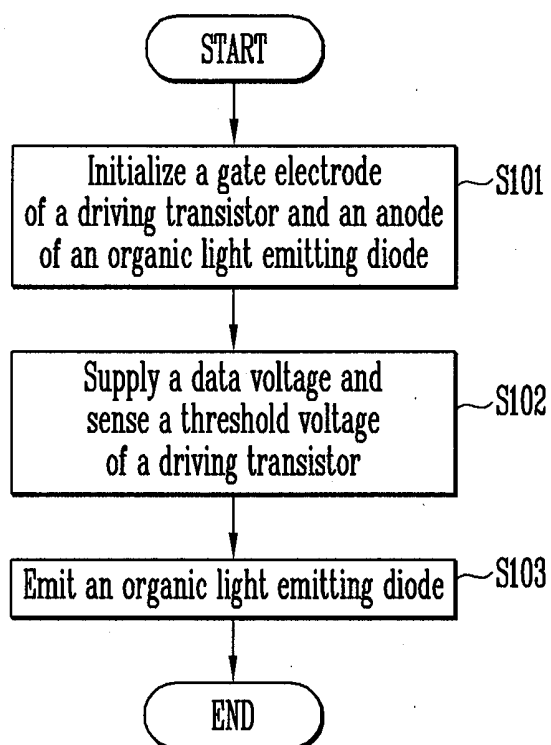


FIG. 6



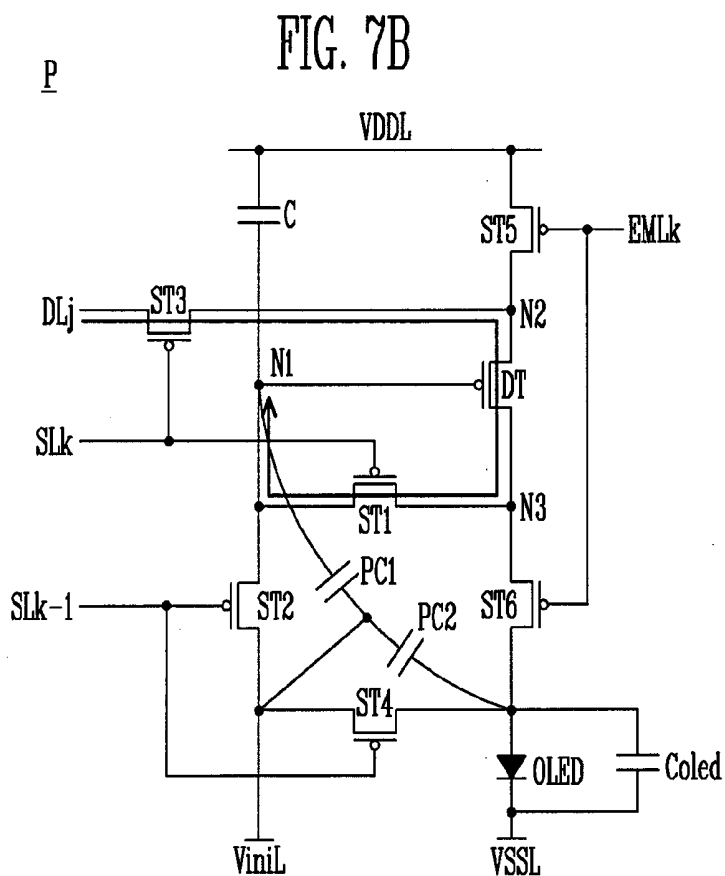
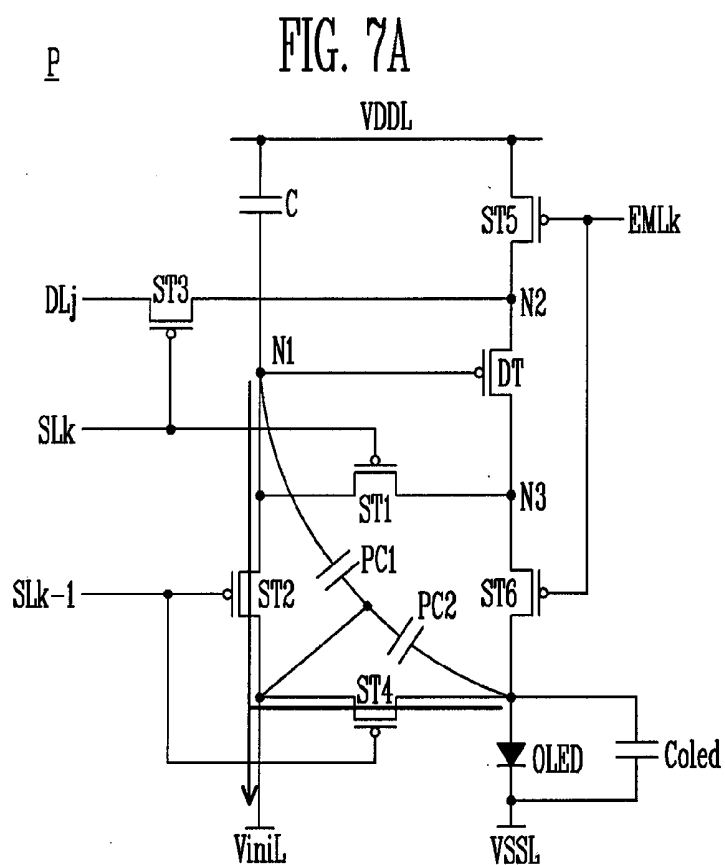


FIG. 7C

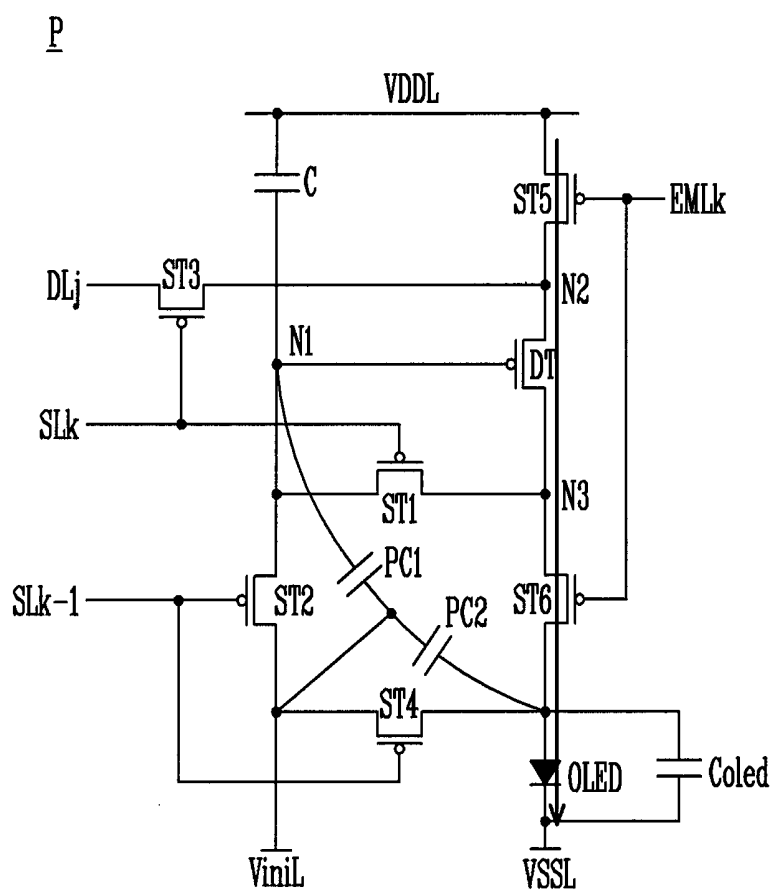


FIG. 8

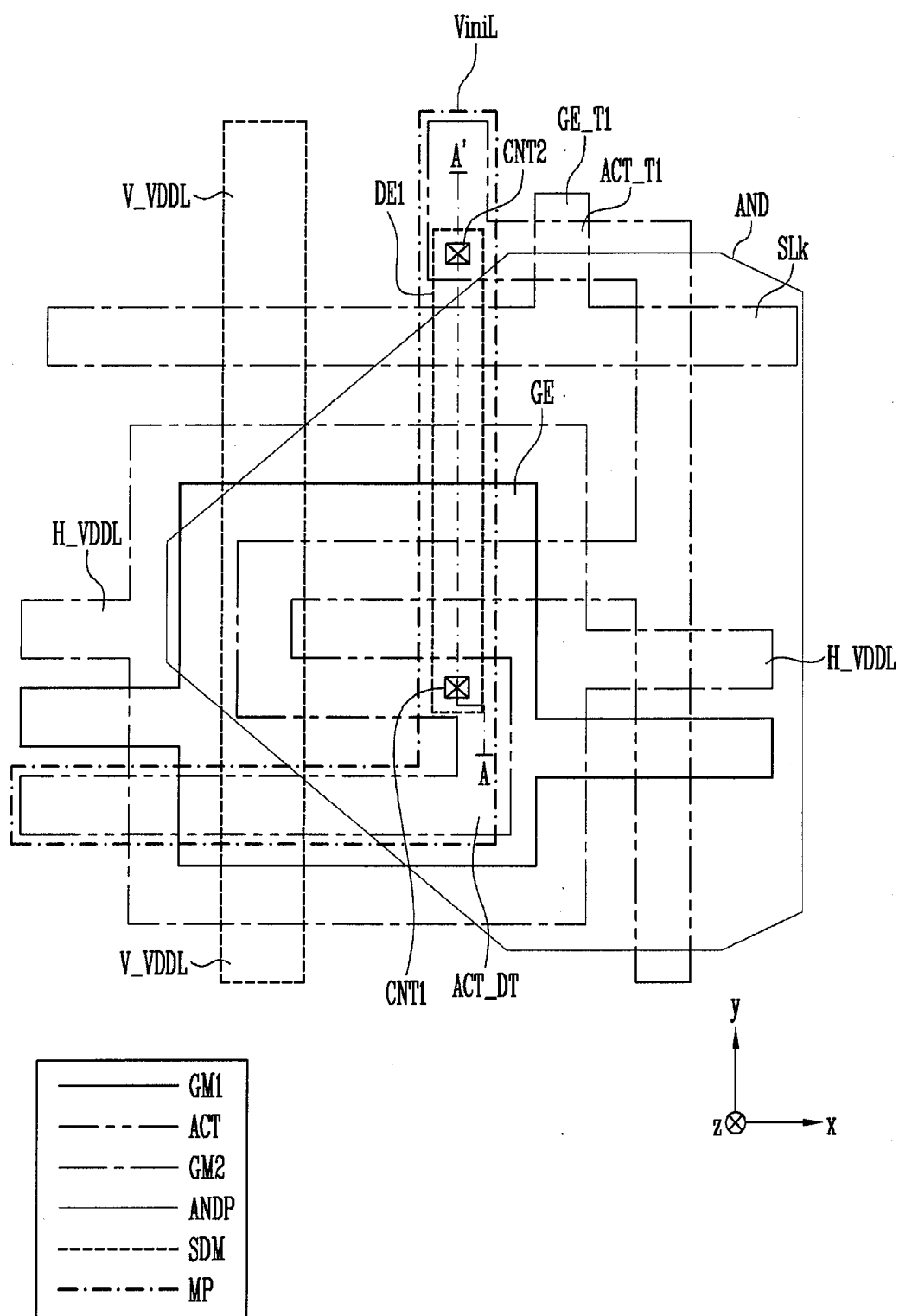
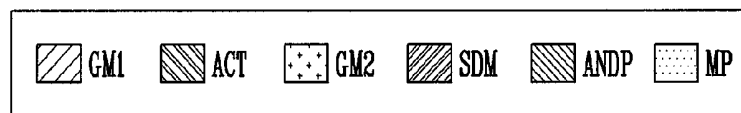
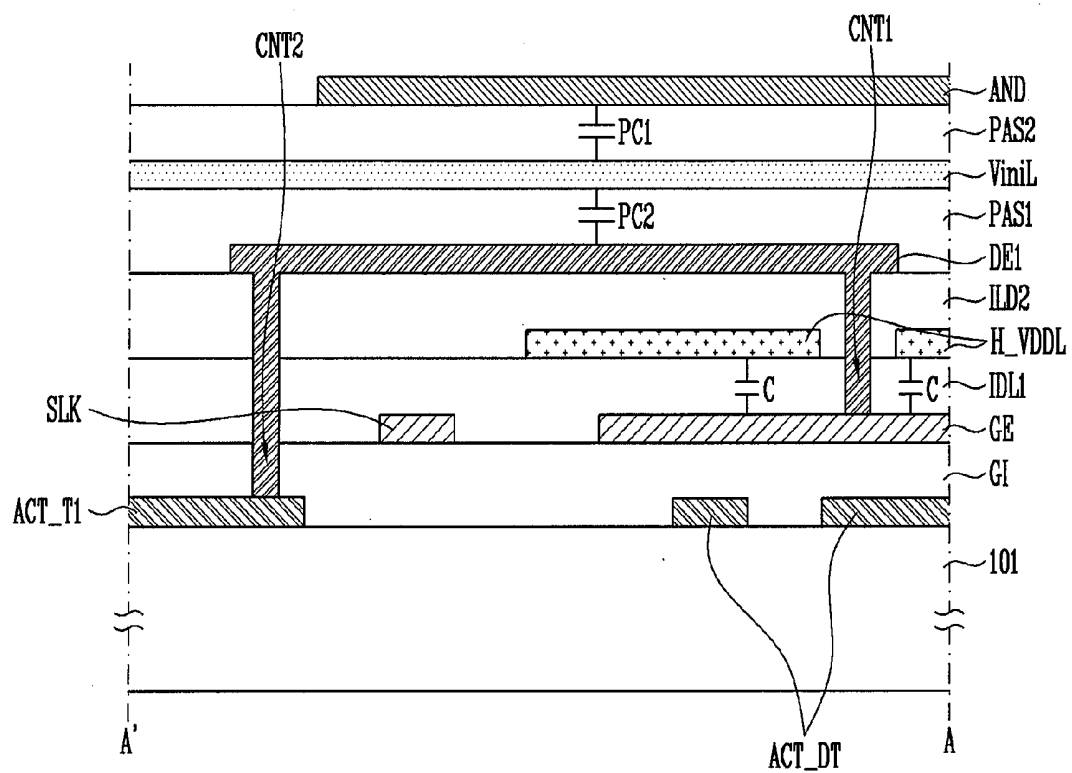


FIG. 9



## ORGANIC LIGHT EMITTING DISPLAY DEVICE

### CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2014-0021786, filed on Feb. 25, 2014, in the Korean Intellectual Property Office, the entire contents of which are incorporated herein by reference.

### BACKGROUND

[0002] 1. Field

[0003] Aspects of embodiments of the present invention relate to an organic light emitting display device.

[0004] 2. Description of the Related Art

[0005] With the development of an information-driven society, the demand for various types of display devices for displaying an image is increasing. Various flat panel displays such as liquid crystal displays (LCDs), plasma display panels (PDPs), and organic light emitting diode (OLED) displays have been widely used in recent years. Among the flat panel displays, OLED displays are driven at a relatively low voltage, are relatively thin, have a relatively wide viewing angle, and have a relatively quick response speed.

[0006] A display panel of the OLED display may include a plurality of pixels arranged in a matrix form. Each of the pixels may include a scan transistor for supplying a data voltage of a data line in response to a scan signal of a scan line and a driving transistor for adjusting the amount of the current supplied to an organic light emitting diode in accordance with a voltage supplied to a gate electrode. The drain-to-source current  $I_{ds}$  of the driving transistor supplied to the organic light emitting diode can be expressed according to the following equation:

$$I_{ds} = k(V_{gs} - V_{th})^2 \quad (1)$$

where  $k$  represents a proportionality coefficient determined by the structure and physical properties of the driving transistor,  $V_{gs}$  represents the gate-source voltage of the driving transistor, and  $V_{th}$  represents the threshold voltage of the driving transistor.

[0007] The drain-to-source current  $I_{ds}$  of the driving transistor depends upon the threshold voltage  $V_{th}$  of the driving transistor. However, the threshold voltage  $V_{th}$  of the driving transistor may differ (or vary) due to process error (e.g., variability in the manufacturing processes). Alternatively, the threshold voltage  $V_{th}$  of the driving transistor may shift or change as the driving transistor degrades (or ages) over time. Therefore, the threshold voltage  $V_{th}$  of the driving transistor may differ from pixel to pixel. As a result, the luminance of light emitted from each of the pixels may differ even if the same data voltage is supplied to the pixels.

### SUMMARY

[0008] Aspects of embodiments of the present invention include an organic light emitting display device and a method for driving the same, which may compensate for the threshold voltage of the driving transistor and reduce or minimize the luminance difference between pixels of a display panel.

[0009] According to an aspect of an embodiment of the present invention, an organic light emitting display device includes a display panel including data lines, scan lines, a first power voltage line supplying a first power voltage, and a

plurality of pixels, a pixel of the plurality pixels including: a driving transistor configured to control an amount of a drain-to-source current flowing from a first electrode of the driving transistor to a second electrode of the driving transistor according to a voltage applied to a gate electrode of the driving transistor; an organic light emitting diode configured to emit light in accordance with the drain-to-source current; and a first transistor having a gate electrode coupled to a scan line of the scan lines, a first electrode coupled to the second electrode of the driving transistor, and a second electrode coupled to the gate electrode of the driving transistor, wherein the first power voltage line is disposed between the second electrode of the first transistor and an anode of the organic light emitting diode.

[0010] The scan lines and the gate electrode of the driving transistor may be formed as a first metal pattern, the data lines and the second electrode of the first transistor may be formed as a second metal pattern, the first power voltage line may be formed as a third metal pattern, and wherein the anode of the organic light emitting diode may be formed as a fourth metal pattern.

[0011] A length of the first power voltage line along a first direction may be longer than a length of the second electrode of the first transistor along the first direction, and a length of the first power voltage line along a second direction may be longer than a length of the second electrode of the first transistor along the second direction.

[0012] The second electrode of the first transistor may be coupled to the gate electrode of the driving transistor through a first contact hole.

[0013] The second electrode of the first transistor may be coupled to an active layer of the first transistor through a second contact hole.

[0014] The first contact hole may penetrate a plurality of insulator layers and the second contact hole may penetrate a gate insulator and the plurality of insulator layers.

[0015] The pixel may further include: a second transistor including a gate electrode coupled to another scan line of the scan lines, a first electrode coupled to the gate electrode of the driving transistor, and a second electrode coupled to the first power voltage line; a third transistor including a gate electrode coupled to the scan line, a first electrode coupled to a data line, and a second electrode coupled to the first electrode of the driving transistor; and a fourth transistor including a gate electrode coupled to the another scan line, a first electrode coupled to the anode of the organic light emitting diode, and a second electrode coupled to the first power voltage line.

[0016] The display panel may further include a plurality of emission lines.

[0017] The pixel may further include: a fifth transistor including a gate electrode coupled to an emission line of the emission lines, a first electrode coupled to a second power voltage line supplying a second power voltage, and a second electrode coupled to the first electrode of the driving transistor; and a sixth transistor including a gate electrode coupled to the emission line, a first electrode coupled to the second electrode of the driving transistor, and a second electrode coupled to the anode of the organic light emitting diode.

[0018] The pixel may further include a capacitor coupled between the gate electrode of the driving transistor and the second power voltage line.

[0019] A cathode of the organic light emitting diode may be coupled to a third power voltage line configured to supply a third power voltage.

[0020] The display panel may be configured to: supply a scan signal to the scan line, the scan signal having a gate on voltage during a first period, supply another scan signal to the another scan line, the another scan signal having a gate on voltage during a second period, and supply an emission signal to the emission line, the emission signal having a gate on voltage during a third period.

[0021] The display panel may be configured to change the second power voltage.

[0022] The third power voltage may have a first voltage in a normal mode and a second voltage in a black grayscale mode.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will convey the scope of embodiments of the present invention to those skilled in the art.

[0024] In the drawing figures, dimensions may be exaggerated for clarity of illustration. It will be understood that when an element is referred to as being “between” two elements, it can be the only element between the two elements, or one or more intervening elements may also be present. Like reference numerals refer to like elements throughout.

[0025] FIG. 1 is a circuit diagram showing an example of a first parasitic capacitance between a gate electrode of a driving transistor and an anode of an organic light emitting diode, and a second parasitic capacitance between the anode of the organic light emitting diode and a low voltage line.

[0026] FIG. 2 is a block diagram schematically showing an organic light emitting display device according to an example embodiment of the present invention.

[0027] FIG. 3 is an equivalent circuit diagram of a pixel according to an example embodiment of the present invention.

[0028] FIG. 4 is a circuit diagram showing an example of a first parasitic capacitance between a gate electrode of a driving transistor and an anode of an organic light emitting diode, and second and third parasitic capacitances between the anode of the organic light emitting diode and a low voltage line according to an example embodiment of the present invention.

[0029] FIG. 5 is a waveform diagram showing signals which, according to one embodiment of the present invention, are input into a pixel of FIG. 3.

[0030] FIG. 6 is a flow chart illustrating a method for driving a pixel of FIG. 3 according to one embodiment of the present invention.

[0031] FIGS. 7A, 7B, and 7C are circuit diagrams of a pixel of FIG. 3 during first, second, and third periods according to one embodiment of the present invention.

[0032] FIG. 8 is a plan view illustrating an example of a driving transistor and a first transistor of FIG. 3 according to one embodiment of the present invention.

[0033] FIG. 9 is a cross-sectional diagram along A-A' of FIG. 8 according to one embodiment of the present invention.

#### DETAILED DESCRIPTION

[0034] Hereinafter, certain exemplary embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when a first element is described as being coupled to a second element, the first element may be not only directly coupled to the second element but may also be indirectly coupled to the second element via a third element. Further, some of the elements that are not essential to the complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0035] FIG. 1 is a circuit diagram showing an example of a first parasitic capacitance between a gate electrode of a driving transistor and an anode of an organic light emitting diode, and a second parasitic capacitance between the anode of the organic light emitting diode and a low voltage line according to a related art. Referring to FIG. 1, the first parasitic capacitance PC is formed between the gate electrode GE of the driving transistor and the anode AND of the organic light emitting diode. The second parasitic capacitance Coled is formed between the anode AND of the organic light emitting diode and a low power voltage line VSSL supplying a low power voltage.

[0036] In some related art, changes are made to the low power voltage to a power consumption of a display panel. In this case, a voltage change of the low power voltage may be applied to the anode AND of the organic light emitting diode through the second parasitic capacitance Coled. Thus, a voltage of the anode AND of the organic light emitting may be changed. Also, a voltage change of the anode AND may be applied to the gate electrode GE of the driving transistor through the first parasitic capacitance PC. Thus, a voltage of the gate electrode GE of the driving transistor may be changed.

[0037] Therefore, the voltage of the gate electrode GE of the driving transistor may change through the first and second parasitic capacitances PC and Coled when the low power voltage is changed. As a result, the organic light emitting diode may emit a light (or an amount of light) different from an originally intended light (or amount of light).

[0038] The embodiments of the invention may prevent (or reduce) the voltage change of the gate electrode GE of the driving transistor through the first and second parasitic capacitances PC and Coled when the low power voltage is changed. Hereinafter, the embodiments of the invention are described in detail with reference to FIGS. 2, 3, 4, 5, 6, 7A, 7B, 7C, and 8.

[0039] FIG. 2 is a block diagram schematically showing an organic light emitting display device according to one embodiment. Referring to FIG. 2, the organic light emitting display device according to one embodiment includes a display panel 10, a data driver 20, a scan driver 30, a timing controller 40, and a power supply unit 50.

[0040] Data lines D1 to Dm and scan lines SL1 to SLn crossing each other are formed in the display panel 10, wherein m is a positive integer greater than or equal to 2 and n is a positive integer greater than or equal to 2. Also, emission lines EML1 to EMLn may be formed in the display panel. The emission lines EML1 to EMLn may extend along a direction parallel to the scan lines SL1 to SLn. Also, pixels P are arranged in a matrix form in the display panel 10. A pixel P according to one embodiment is described in conjunction with FIG. 3.

[0041] The data driver 20 includes at least one source drive IC. The source drive IC receives digital video data DATA from the timing controller 40. The source drive IC converts the digital video data DATA into data voltages in response to a source timing control signal DCS from the timing controller 40. The source drive IC supplies the data voltages to the data lines D1 to Dm of the display panel 10 in synchronization with scan signals. Therefore, the data voltages are supplied to pixels to which a scan signal is supplied.

[0042] The scan driver 30 includes a scan signal output part and an emission signal output part. Each of the scan signal output part and the emission signal output part may have a shift register for sequentially outputting signals, a level shifter for shifting the signals of the shift register to a swing width suitable for transistors of the pixels, a buffer, and the like.

[0043] The scan signal output part may sequentially output the scan signals SCAN to the scan lines SL1 to SLn of the display panel 10. The emission signal output part may sequentially output emission signals EM to the emission lines EML1 to EMLn of the display panel 10. The scan signal SCAN and the emission signal EM are described in more detail in conjunction with FIG. 4.

[0044] According to one embodiment, the timing controller 40 receives the digital video data DATA from a host system through a low voltage differential signaling (LVDS) interface, a transition minimized differential signaling (TMDS) interface, etc. The timing controller 40 may receive timing signals such as a vertical synchronization signal, a horizontal synchronization signal, a data enable signal, and a dot clock, and may generate timing control signals for controlling operation timings of the data driver 20 and scan driver 30 based on the timing signals. The timing control signals include a scan timing control signal SCS for controlling the operation timing of the scan driver 30 and a data timing control signal DCS for controlling the operation timing of the data driver 20. The timing controller 40 outputs the scan timing control signal SCS to the scan driver 30, and outputs the data timing control signal DCS and the digital video data DATA to the data driver 20.

[0045] The power supply unit 50 supplies a first power voltage to the pixels P through first power voltage line ViniL, a second power voltage to the pixels P through the second power voltage line VDDL, and a third power voltage to the pixels P through the third power voltage line VSSL. The first power voltage may be an initialization voltage, the second power voltage may be a high power voltage, and the third power voltage may be a low power voltage. Also, the power supply unit 50 may supply a gate on voltage Von and a gate off voltage Voff to the scan driver 30. The gate on voltage Von refers to a voltage for turning on transistors of the pixels P, and the gate off voltage Voff refers to a voltage for turning off the transistors of the pixels P.

[0046] The power supply unit 50 may change the third power voltage to reduce a power consumption of the display panel 10. The timing controller 40 may generate a mode signal and output the mode signal to the power supply unit 50. For example, the timing controller 40 may control the power supply unit 50 to operate in a normal mode when the mode signal has a first logic level voltage and to operate in a black grayscale mode when the mode signal has a second logic level voltage.

[0047] The power supply unit 50 may supply the third power voltage depending on the mode signal. For example, the power supply unit 50 may supply the third power voltage

as a first voltage in the normal mode. The power supply unit 50 may supply the third power voltage as a second voltage higher than the first voltage in a black grayscale mode in which the pixels P emit light in accordance with a black grayscale (e.g., a grayscale image). The voltage change of the gate electrode of the driving transistor when the third power voltage is changed is described in more detail with reference to FIG. 4.

[0048] FIG. 3 is an equivalent circuit diagram of a pixel according to one embodiment. Referring to FIG. 3, the pixel P according to one embodiment is coupled to a scan line, another scan line, a data line, and an emission line. For example, the pixel P may be coupled to a (k-1)-th scan line SLk-1, a k-th scan line SLk, a k-th emission line EMLk, and a j-th data line Dj, wherein k is a positive integer greater than or equal to 2 and less than or equal to n, and j is a positive integer greater than or equal to 1 and less than or equal to m. Also, the pixel P according to one embodiment is coupled to first, second, and third power voltage lines ViniL, VDDL, and VSSL.

[0049] The pixel P according to one embodiment includes a driving transistor DT, an organic light emitting diode OLED, switch elements, and a capacitor C. The switch elements include first, second, third, fourth, fifth, and sixth transistors ST1, ST2, ST3, ST4, ST5, and ST6.

[0050] The driving transistor DT controls an amount of drain-to-source current Ids flowing from a first electrode thereof to a second electrode thereof according to a voltage applied to a gate electrode of the driving transistor DT. The drain-to-source current Ids of the driving transistor DT is proportional to the square of a difference between the gate-source voltage Vgs of the driving transistor and the threshold voltage Vth of the driving transistor as described in equation 1 above. A gate electrode of the driving transistor DT is coupled to a first node N1, a first electrode thereof is coupled to a second node N2, and a drain electrode thereof is coupled to a third node N3. Here, the first electrode may be a source or a drain electrode, and the second electrode may be a different electrode from the first electrode (e.g., the second electrode may be the drain or the source electrode). For example, if the first electrode is the source electrode, then the second electrode is the drain electrode.

[0051] The organic light emitting diode OLED emits light in accordance with the drain-to-source current Ids of the driving transistor (or TFT) DT. The luminance of light emitted by the organic light emitting diode OLED is proportional to the drain-to-source current Ids of the driving transistor DT. An anode of the organic light emitting diode OLED is coupled to a second electrode of the sixth transistor ST6 and a first electrode of the fourth transistor ST4. A cathode of the organic light emitting diode OLED is coupled to the third power voltage line VSSL supplying the third power voltage.

[0052] The first transistor ST1 is coupled between the first node N1 and the third node N3. The first transistor ST1 is turned on by the scan signal from the k-th scan line SLk. When the first transistor ST1 is turned on, the first node N1 is coupled to the third node N3, thus the driving transistor DT is diode-coupled. A gate electrode of the first transistor ST1 is coupled to the k-th scan line SLk, a first electrode thereof is coupled to the third node N3, and a second electrode thereof is coupled to the first node N1.

[0053] The second transistor ST2 is coupled between the first node N1 and the first power voltage line ViniL supplying the first power voltage. The second transistor ST2 is turned on

by a scan signal from the (k-1)-th line SLk-1. When the second transistor ST2 is turned on, the first node N1 is coupled to the first power voltage line ViniL, thus the first node N1 is initialized to the first power voltage. A gate electrode of the second transistor ST2 is coupled to the (k-1)-th scan line SLk-1, a first electrode thereof is coupled to the first node N1, and a second electrode thereof is coupled to the first power voltage line ViniL.

[0054] The third transistor ST3 is coupled between the second node N2 and the j-th data line DLj. The third transistor ST3 is turned on by the scan signal from the k-th scan line SLk. When the third transistor ST3 is turned on, the second node N2 is coupled to the data line DL, thus a data voltage Vdata from the j-th data line DLj is supplied to the second node N2. A gate electrode of the third transistor ST3 is coupled to the k-th scan line SLk, a first electrode thereof is coupled to the j-th data line DLj, and a second electrode thereof is coupled to the second node N2.

[0055] The fourth transistor ST4 is coupled between the anode of the organic light emitting diode OLED and the first power voltage line ViniL. The fourth transistor ST4 is turned on by the scan signal from the (k-1)-th scan line. When the fourth transistor ST4 is turned on, the anode of the organic light emitting diode OLED is coupled to the first power voltage line ViniL, thus the anode of the organic light emitting diode OLED is initialized to the first power voltage. A gate electrode of the fourth transistor ST4 is coupled to the (k-1)-th scan line SLk-1, a first electrode thereof is coupled to the anode of the organic light emitting diode OLED, and a second electrode thereof is coupled to the first power voltage line ViniL.

[0056] The fifth transistor ST5 is coupled between the second node N2 and the second power voltage line VDDL supplying a second power voltage. The fifth transistor ST5 is turned on by an emission signal from the k-th emission line EMLk. When the fifth transistor ST5 is turned on, the second node N2 is coupled to the second power voltage line VDDL, thus the second power voltage is supplied to the second node N2. A gate electrode of the fifth transistor ST5 is coupled to the k-th emission line EMLk, a first electrode thereof is coupled to the second power voltage line VDDL, and a second electrode thereof is coupled to the second node N2.

[0057] The sixth transistor ST6 is coupled between the third node N3 and the anode of the organic light emitting diode OLED. The sixth transistor ST6 is turned on by the emission signal from the k-th emission line EMLk. When the sixth transistor ST6 is turned on, the third node N3 is coupled to the anode of the organic light emitting diode OLED. A gate electrode of the sixth transistor ST6 is coupled to the k-th emission line EMLk, a first electrode thereof is coupled to the third node N3, and a second electrode thereof is coupled to the anode of the organic light emitting diode OLED. When the fifth and sixth transistors are turned-on, the drain-to-source current Ids of the driving transistor DT is supplied to the organic light emitting diode OLED.

[0058] The capacitor C is formed between the first node N1 and the second power voltage line VDDL. The capacitor C may store a difference voltage between a voltage of the first node N1 and the second power voltage.

[0059] A first parasitic capacitance PC1 is formed between the gate electrode of the driving transistor DT and the first power voltage line ViniL. A second parasitic capacitance PC2 is formed between the anode AND of the organic light emitting diode and the first power voltage line ViniL. A third

parasitic capacitance Coled is formed between the anode AND of the organic light emitting diode and the third power voltage line VSSL.

[0060] The first node N1 is a gate node coupled to the gate electrode of the driving transistor DT. The first node N1 is a contact point at which the gate electrode of the driving transistor DT, the second electrode of the first transistor ST1 and the first electrode of the third transistor ST2 are each mutually electrically coupled. The second node N2 is a source node coupled to the first electrode of the driving transistor DT. The second node N2 is a contact point at which the first electrode of the driving transistor DT, the second electrode of the third transistor ST3, and the second electrode of the fifth transistor ST5 are each mutually electrically coupled. The third node N3 is a drain node coupled to the second electrode of the driving transistor DT. The third node N3 is a contact point at which the second electrode of the driving transistor DT, the first electrode of the first transistor ST1, and the first electrode of the sixth transistor ST6 are each mutually electrically coupled.

[0061] Active layers of the first, second, third, fourth, fifth, and sixth transistors ST1, ST2, ST3, ST4, ST5, and ST6 and the driving transistor DT have been described as being formed of Poly-Si by a low temperature Poly-Si (LTPS) process. The active layers refer to semiconductor layers. However, the embodiments are not limited thereto, and the active layers of the first, second, third, fourth, fifth, and sixth transistors ST1, ST2, ST3, ST4, ST5, and ST6 and the driving transistor DT may be formed of either a-Si or an oxide semiconductor, or other suitable semiconductor material.

[0062] Also, one embodiment has been described in which the first, second, third, fourth, fifth, and sixth transistors ST1, ST2, ST3, ST4, ST5, and ST6 and the driving transistor DT are implemented as P-type transistors. However, embodiments of the present invention are not limited thereto, and the first, second, third, fourth, fifth, and sixth transistors ST1, ST2, ST3, ST4, ST5, and ST6 and the driving transistor DT may be implemented as N-type transistors. When the first, second, third, fourth, fifth, and sixth transistors ST1, ST2, ST3, ST4, ST5, and ST6 and the driving transistor DT are implemented as N-type transistors, a waveform diagram shown in FIG. 5 may be modified in accordance with the characteristics of the N-type transistors.

[0063] The first, second, and third power voltages are set after consideration of the characteristics of the driving transistor DT and the first, second, third, fourth, fifth, and sixth transistors ST1, ST2, ST3, ST4, ST5, and ST6, the characteristics of the organic light emitting diode OLED, and so on.

[0064] In addition, according to one embodiment the third power voltage may be changed to reduce a power consumption of the display panel. For example, one embodiment may supply the third power voltage as a first voltage in the normal mode and supply the third power voltage as a second voltage higher than the first voltage in a black grayscale mode. The voltage change of the gate electrode of the driving transistor when the third power voltage is changed is described in more detail with reference to FIG. 4.

[0065] FIG. 4 is a circuit diagram showing an example of first and second parasitic capacitances between a gate electrode of a driving transistor and an anode of an organic light emitting diode, and a third parasitic capacitance between the anode of the organic light emitting diode and a low voltage line according to one embodiment. Referring to FIG. 4, the first parasitic capacitance PC1 is formed between the gate

electrode GE of the driving transistor and the first power voltage line ViniL. The second parasitic capacitance PC2 is formed between the anode AND of the organic light emitting diode and the first power voltage line ViniL. The third parasitic capacitance Coled is formed between the anode AND of the organic light emitting diode and the third power voltage line VSSL.

[0066] When the third power voltage is changed, a voltage change of the third power voltage may be applied to the anode AND of the organic light emitting diode through the third parasitic capacitance Coled. Thus, a voltage of the anode AND of the organic light emitting diode may be changed. However, the first power voltage is not influenced by the voltage change of the anode AND of the organic light emitting diode because the first power voltage is a direct current (DC) voltage. Therefore, the voltage of the gate electrode GE of the driving transistor is not influenced by the voltage change of the anode AND of the organic light emitting diode. As a result, one embodiment may prevent or reduce the voltage change of the gate electrode GE of the driving transistor due to the parasitic capacitances of the pixel P when the third power voltage (e.g., the voltage supplied to third voltage power line VSSL) is changed.

[0067] FIG. 5 is a waveform diagram showing signals which are input into a pixel of FIG. 3. FIG. 5 depicts a (k-1)-th scan signal SCANk-1 of the (k-1)-th scan line SLk-1, a k-th scan signal SCANk of the k-th scan line SLk, and a k-th emission signal EMk of the k-th emission line EMLk during q-th and (q+1)-th frame periods FRq and FRq+1, wherein q is a positive integer.

[0068] Referring to FIG. 5, the (k-1)-th scan signal SCANk-1 is for controlling the second and fourth transistors ST2 and ST4, the k-th scan signal SCANk is for controlling the first and third transistors ST1 and ST3, and the k-th emission signal EMk is for controlling the fifth and sixth transistors ST5 and ST6. Each scan signal and each emission signal may have a cycle of one frame period.

[0069] Each scan signal may have the gate on voltage Von during one horizontal period. One horizontal period refers to a period that supplies data voltages to pixels arranged on a horizontal line. Here, the pixels arranged on a horizontal line refer to pixels coupled to one scan line. The data voltages are supplied in synchronized with the gate on voltage Von of each scan signal.

[0070] One frame period includes first, second, and third periods t1, t2, and t3. The first period t1 is a period that initializes the gate electrode of the driving transistor DT and the anode of the organic light emitting diode OLED. The second period t2 is a period that supplies a data voltage to the first node N1 and senses a threshold voltage of the driving transistor DT. The third period t3 is a period that emits light from an organic light emitting diode OLED depending on the drain-to-source current Ids of the driving transistor DT.

[0071] The (k-1)-th scan signal SCANk-1 may have the gate on voltage Von during the first period t1 and the gate off voltage Voff during the second and third periods t2 and t3. The k-th scan signal SCANk may have the gate on voltage Von during the second period t3 and the gate off voltage Voff during the first and third periods t1 and t3. The k-th emission signal may have the gate on voltage Von during the third period t3 and the gate off voltage Voff during the first and second periods t2 and t3. The gate on voltage Von refers to a voltage for turning on first, second, third, fourth, fifth, and sixth transistors ST1, ST2, ST3, ST4, ST5, and ST6, and the

gate off voltage Voff refers to a voltage for turning off the first, second, third, fourth, fifth, and sixth transistors ST1, ST2, ST3, ST4, ST5, and ST6.

[0072] FIG. 6 is a flow chart illustrating a method for driving a pixel of FIG. 3. FIGS. 7A, 7B, and 7C are circuit diagrams of a pixel of FIG. 3 during first, second, third, and fourth periods. The method for driving the pixel P of FIG. 3 during the first, second, and third periods t1, t2, and t3 is described in detail in conjunction with FIGS. 5, 6 7A, 7B, and 7C.

[0073] First, as shown in FIG. 5, during the first period t1, the (k-1)-th scan signal SCANk-1 having the gate on voltage Von is supplied to the pixel P. The k-th scan signal SCANk having the gate off voltage Voff and the k-th emission signal EMk having the gate off voltage Voff are supplied to the pixel P during the first period t1.

[0074] Referring to FIG. 7A, the second and fourth transistors ST2 and ST4 are turned on by the (k-1)-th scan signal SCANk-1 having the gate on voltage Von. The first and third transistors ST1 and ST3 are turned off by the k-th scan signal SCANk having the gate off voltage Voff. The fifth and sixth transistors ST5 and ST6 are turned off by the k-th emission signal EMk having the gate off voltage Voff.

[0075] The first node N1 is initialized to the first power voltage of the first power voltage line ViniL because the second transistor ST2 is turned on during the first period t1. Also, the anode of the organic light emitting diode OLED is initialized to the first power voltage of the first power voltage line ViniL because the fourth transistor ST4 is turned on during the first period t1. The first power voltage may be substantially same as the third power voltage to prevent the organic light emitting diode OLED from emitting light. (See S101 in FIG. 6)

[0076] Second, as shown in FIG. 5, during the second period t2, the k-th scan signal SCANk having the gate on voltage Von is supplied to the pixel P. The (k-1)-th scan signal SCANk-1 having the gate off voltage Voff and the k-th emission signal EMk having the gate off voltage Voff are supplied to the pixel P during the second period t2.

[0077] Referring to FIG. 7B, the first and third transistors ST1 and ST3 are turned on by the k-th scan signal SCANk having the gate on voltage Von. The second and fourth transistors ST2 and ST4 are turned off by the (k-1)-th scan signal SCANk-1 having the gate off voltage Voff. The fifth and sixth transistors ST5 and ST6 are turned off by the k-th emission signal EMk having the gate off voltage Voff.

[0078] The first node N1 is electrically coupled to the third node N3 because the first transistor ST1 is turned on, thus the driving transistor DT is diode-coupled. Also, the second node N2 is electrically coupled to the j-th data line Dj because the second transistor ST2 is turned on, thus a data voltage of the j-th data line Dj is supplied to the second node N2.

[0079] The drain-to-source current Ids of the driving transistor DT flows until the gate-source voltage of the driving transistor DT reaches the threshold voltage of the driving transistor DT because the gate-source voltage "Vini-Vdata" is less than the threshold voltage of the driving transistor DT. Therefore, the voltage of the first node N1 rises up to "Vdata+Vth". The voltage "Vdata+Vth" of the first node N1 is stored in the capacitor C. For example, the threshold voltage of the driving transistor DT may be sensed by the capacitor C during the second period t2. Vini refers to the first power voltage and Vdata refers to the data voltage and Vth refers to the threshold voltage of the driving transistor DT. (See S102 in FIG. 6)

**[0080]** Third, as shown in FIG. 5, during the third period t3, the k-th emission signal EMk having the gate on voltage Von are supplied to the pixel P. The (k-1)-th scan signal SCANk-1 having the gate off voltage Voff and the k-th scan signal SCANk having the gate off voltage Voff are supplied to the pixel P during the third period t3.

**[0081]** Referring to FIG. 7C, the fifth and sixth transistors ST5 and ST6 are turned on by the k-th emission signal EMk having the gate on voltage Von. The second and fourth transistors ST2 and ST4 are turned off by the (k-1)-th scan signal SCANk-1 having the gate off voltage Voff. The first and third transistors ST1 and ST3 are turned off by the k-th scan signal SCANk having the gate off voltage Voff.

**[0082]** The second node N2 is electrically coupled to the second power voltage line VDDL because the fifth transistor ST5 is turned on. The third node N3 is electrically coupled to the anode of the organic light emitting diode OLED because the sixth transistor ST6 is turned on. Therefore, the drain-to-source current Ids of the driving transistor DT is supplied to the organic light emitting diode OLED. Because the voltage "Vdata+Vth" of the first node N1 is stored to the capacitor C, the drain-to-source current Ids of the driving transistor DT is expressed in following equation:

$$I_{ds}=k' \cdot (V_{gs}-V_{th})^2=k' \cdot ((V_{data}+V_{th})-ELVDDL-V_{th})^2 \quad (2)$$

where k' represents a proportionality coefficient determined by the structure and physical properties of the driving transistor DT, Vgs represents the gate-source voltage of the driving transistor DT, Vth represents the threshold voltage of the driving transistor DT, Vdata represents the data voltage, and Vdd represents the second power voltage. The gate voltage Vg of the driving transistor DT is Vdata+Vth, and the source voltage Vs of the driving transistor DT is Vdd during the third period t3. To sum up equation 2, the drain-to-source current Ids of the driving transistor DT is derived as expressed in the following equation:

$$I_{ds}=k' \cdot (V_{data}-ELVDDL)^2 \quad (3)$$

**[0083]** Therefore, the drain-to-source current Ids does not depend on the threshold voltage of the driving transistor DT as in equation 3. Therefore, one embodiment of the present invention may compensate the threshold voltage Vth of the driving transistor DT. (See S103 in FIG. 6)

**[0084]** Accordingly, one embodiment may compensate the threshold voltage Vth of the driving transistor DT. As a result, one embodiment may reduce or minimize the luminance difference between pixels of a display panel because the drain-to-source current Ids does not depend on the threshold voltage of the driving transistor DT.

**[0085]** FIG. 8 is a plan view illustrating an example of a driving transistor and a first transistor of FIG. 3. FIG. 9 is a cross-sectional diagram of A-A' of FIG. 8. Hereinafter, the connection of a gate electrode GE of the driving transistor DT, a second electrode DE1 of the first transistor ST1 and an active layer ACT\_ST1 of the first transistor ST1 is described in detail with reference to FIGS. 8 and 9.

**[0086]** Referring to FIGS. 8 and 9, an active pattern ACT including an active layer of the driving transistor DT and the active layer ACT\_ST1 of the first transistor ST1 is formed on a lower substrate 101 of the display panel 10. Alternatively, the active pattern ACT may be formed on a buffer layer on the lower substrate 101. The active pattern ACT may be formed of one of a poly-silicon, a-Si, and oxide, and the like.

**[0087]** A gate insulator GI is formed on the active pattern ACT. The gate insulator GI may be formed of SiNx (silicon nitride).

**[0088]** A first gate metal pattern GM1 including the gate electrode GE of the driving transistor DT, a k-th scan line SLk and a gate electrode GE\_ST1 of the first transistor ST1 is formed on the gate insulator GI. The first gate metal pattern GM1 is isolated from the active pattern ACT by the gate insulator GI. The first metal pattern GM1 may be formed of Mo (molybdenum).

**[0089]** A first layer insulator ILD1 is formed on the first gate metal pattern GM1. The first layer insulator ILD1 may be formed of SiNx (silicon nitride).

**[0090]** A second gate metal pattern GM2 including a horizontal second power voltage line H\_VDDL is formed on the first layer insulator ILD1. The second gate metal pattern GM2 is isolated from the first gate metal pattern GM1 by the first layer insulator ILD1.

**[0091]** A second layer insulator ILD2 is formed on the second gate metal pattern GM2. The second layer insulator ILD2 may be formed as a double layer having a SiNx (silicon nitride) layer and a SiO2 (silicon dioxide) layer.

**[0092]** A source/drain metal pattern SDM including a vertical second power voltage line V\_VDDL and the second electrode DE1 of the first transistor ST1 is formed on the second layer insulator ILD2. The source/drain metal pattern SDM is isolated from the second gate metal pattern GM2 by the second layer insulator ILD2. The source/drain metal pattern SDM may be formed as a triple layer having a Ti (Titanium) layer, an Al (Aluminum) layer, and a Ti (Titanium) layer.

**[0093]** In addition, the second electrode DE1 of the first transistor ST1 is coupled to the gate electrode GE of the driving transistor DT through a first contact hole CNT1. The first contact hole CNT1 penetrates the first and second layer insulators ILD1 and ILD2 to expose the gate electrode GE of the driving transistor DT.

**[0094]** Also, the second electrode DE1 of the first transistor ST1 is coupled to the active layer ACT\_T1 of the first transistor ST1 through a second contact hole CNT2. The second contact hole CNT2 penetrates the gate insulator GI, the first and second layer insulators ILD1 and ILD2 to expose the active layer ACT\_T1 of the first transistor ST1.

**[0095]** Moreover, the second power voltage line VDDL includes the horizontal second power voltage line H\_VDDL and the vertical second power voltage line V\_VDDL. The horizontal second power voltage line H\_VDDL may be parallel to a horizontal direction (x-axis direction). The vertical second power voltage line V\_VDDL may be parallel to a vertical direction (y-axis direction). The horizontal second power voltage line H\_VDDL may be coupled to the vertical second power voltage line V\_VDDL through a third contact hole. The third contact hole penetrates the second layer insulator ILD2 for exposing the horizontal second power voltage line H\_VDDL. Also, the overlapped area between the horizontal second power voltage line H\_VDDL and the gate electrode GE of the driving transistor DT functions as the capacitor C.

**[0096]** A first passivation layer PAS1 is formed on the source/drain metal pattern SDM. According to one embodiment, the first passivation layer PAS1 is formed of polyimide.

**[0097]** A metal pattern MP including the first power voltage line ViniL is formed on the first passivation layer PAS1. The metal pattern MP isolated from the source/drain metal pattern

SDM by the first passivation layer PAS1. The overlapped area between the first power voltage line ViniL and the second electrode DE1 of the first transistor ST1 functions as the second parasitic capacitance PC2.

**[0098]** Furthermore, a horizontal direction (x-axis direction) length of the first power voltage line ViniL is longer than a horizontal direction (x-axis direction) length of the second electrode DE1 of the first transistor ST1. Also, a vertical direction (y-axis direction) length of the first power voltage line ViniL is longer than a vertical direction (y-axis direction) length of the second electrode DE1 of the first transistor ST1. As a result, an electrical coupling such as a parasitic capacitance may not be formed or may be reduced between the anode AND of the organic light emitting diode OLED and the second electrode DE1 of the first transistor ST1.

**[0099]** A second passivation layer PAS2 is formed on the metal pattern MP. According to one embodiment, the second passivation layer PAS2 is formed of polyimide.

**[0100]** An anode pattern ANDP including the anode of the organic light emitting diode OLED is formed on the second passivation layer PAS2. The anode pattern ANDP is isolated from the metal pattern MP by the second passivation layer PAS2. The anode pattern ANDP may be formed as a triple layer having an ITO (indium tin oxide) layer, an Ag (silver) layer, and an ITO (indium tin oxide) layer. The overlapped area between the first power voltage line ViniL and the anode AND of the organic light emitting diode OLED functions as the first parasitic capacitance PC1.

**[0101]** As described above with reference to FIGS. 3, 4, 7A, 7B, 7C, and 8, one embodiment may dispose the first power voltage line ViniL supplying the first power voltage corresponding to a direct current voltage between the anode AND of the organic light emitting diode OLED and the second electrode DE1 of the first transistor ST1. As a result, one embodiment may form the first parasitic capacitance PC1 between the anode AND of the organic light emitting diode OLED and the first power voltage line ViniL, and the second parasitic capacitance PC2 between the second electrode DE1 of the first transistor ST1 and the first power voltage line ViniL. As such, one embodiment may prevent or reduce an electrical coupling such as a parasitic capacitance formed between the anode AND of the organic light emitting diode OLED and the second electrode DE1 of the first transistor ST1.

**[0102]** One embodiment may reduce or prevent the voltage of the gate electrode GE of the driving transistor DT from changing even though the anode AND of the organic light emitting diode OLED is changed due to the third parasitic capacitances Coled when the third power voltage is changed. As such, one embodiment may reduce or prevent the voltage of the gate electrode GE of the driving transistor DT from changing by parasitic capacitances when the third power voltage is changed.

**[0103]** Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art at the time of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various

changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims and equivalents thereof.

What is claimed is:

1. An organic light emitting display device, comprising:
  - a display panel comprising data lines, scan lines, a first power voltage line supplying a first power voltage, and a plurality of pixels, a pixel of the plurality of pixels comprising:
    - a driving transistor configured to control an amount of a drain-to-source current flowing from a first electrode of the driving transistor to a second electrode of the driving transistor according to a voltage applied to a gate electrode of the driving transistor;
    - an organic light emitting diode configured to emit light in accordance with the drain-to-source current; and
    - a first transistor having a gate electrode coupled to a scan line of the scan lines, a first electrode coupled to the second electrode of the driving transistor, and a second electrode coupled to the gate electrode of the driving transistor,
  - wherein the first power voltage line is disposed between the second electrode of the first transistor and an anode of the organic light emitting diode.
2. The organic light emitting display device of claim 1, wherein the scan lines and the gate electrode of the driving transistor are formed as a first metal pattern,
  - wherein the data lines and the second electrode of the first transistor are formed as a second metal pattern,
  - wherein the first power voltage line is formed as a third metal pattern, and
  - wherein the anode of the organic light emitting diode are formed as a fourth metal pattern.
3. The organic light emitting display device of claim 1, wherein a length of the first power voltage line along a first direction is longer than a length of the second electrode of the first transistor along the first direction, and
  - wherein a length of the first power voltage line along a second direction is longer than a length of the second electrode of the first transistor along the second direction.
4. The organic light emitting display device of claim 1, wherein the second electrode of the first transistor is coupled to the gate electrode of the driving transistor through a first contact hole.
5. The organic light emitting display device of claim 4, wherein the second electrode of the first transistor is coupled to an active layer of the first transistor through a second contact hole.
6. The organic light emitting display device of claim 5, wherein the first contact hole penetrates a plurality of insulator layers and the second contact hole penetrates a gate insulator and the plurality of insulator layers.
7. The organic light emitting display device of claim 1, wherein the pixel further comprises:
  - a second transistor including a gate electrode coupled to another scan line of the scan lines, a first electrode coupled to the gate electrode of the driving transistor, and a second electrode coupled to the first power voltage line;
  - a third transistor including a gate electrode coupled to the scan line, a first electrode coupled to a data line, and a second electrode coupled to the first electrode of the driving transistor; and

a fourth transistor including a gate electrode coupled to the another scan line, a first electrode coupled to the anode of the organic light emitting diode, and a second electrode coupled to the first power voltage line.

**8.** The organic light emitting display device of claim **7**, wherein the display panel further comprises a plurality of emission lines.

**9.** The organic light emitting display device of claim **8**, wherein the pixel further comprises:

a fifth transistor including a gate electrode coupled to an emission line of the emission lines, a first electrode coupled to a second power voltage line supplying a second power voltage, and a second electrode coupled to the first electrode of the driving transistor; and

a sixth transistor including a gate electrode coupled to the emission line, a first electrode coupled to the second electrode of the driving transistor, and a second electrode coupled to the anode of the organic light emitting diode.

**10.** The organic light emitting display device of claim **9**, wherein the pixel further comprises a capacitor coupled between the gate electrode of the driving transistor and the second power voltage line.

**11.** The organic light emitting display device of claim **10**, wherein a cathode of the organic light emitting diode is coupled to a third power voltage line configured to supply a third power voltage.

**12.** The organic light emitting display device of claim **10**, wherein the display panel is configured to:

supply a scan signal to the scan line, the scan signal having a gate on voltage during a first period,

supply another scan signal to the another scan line, the another scan signal having a gate on voltage during a second period, and

supply an emission signal to the emission line, the emission signal having a gate on voltage during a third period.

**13.** The organic light emitting display device of claim **11**, wherein the display panel is configured to change the second power voltage.

**14.** The organic light emitting display device of claim **13**, wherein the third power voltage has a first voltage in a normal mode and a second voltage in a black grayscale mode.

\* \* \* \* \*

|                |                                                                              |         |            |
|----------------|------------------------------------------------------------------------------|---------|------------|
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| [标]申请(专利权)人(译) | 三星显示有限公司                                                                     |         |            |
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#### 摘要(译)

一种有机发光显示装置，包括：显示面板，包括数据线，扫描线，提供第一电源电压的第一电源电压线，以及像素，像素的像素包括：驱动晶体管，被配置为控制漏极到 - 源极电流根据驱动晶体管的栅极电压从驱动晶体管的第一电极流到驱动晶体管的第二电极;有机发光二极管 ( OLED )，被配置为根据漏极 - 源极电流发光;第一晶体管，其栅极连接到扫描线的扫描线，第一电极连接到驱动晶体管的第二电极，第二电极连接到驱动晶体管的栅极，第一电源电压线在第一晶体管的第二电极和OLED的阳极之间。

